SYSTEMATIC-ERROR SIGNALS IN THE AC JOSEPHSON VOLTAGE STANDARD: MEASUREMENT AND REDUCTION

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Abstract: We investigate the dominant frequency-dependent systematic error signals (SES) in the ac Josephson voltage standard. We describe our error measurement technique and a number of methods to reduce the errors. Most importantly we found that a small change in on-chip wiring significantly reduced the SES, improved SES measurement stability, and enabled a suitable bias correction method. We demonstrate that reduction of the SES using various techniques greatly improves agreement between the ac-dc differences of the two arrays and improves the absolute ac voltage accuracy.

Keywords: Josephson arrays, quantization, standards, voltage measurement.

1. INTRODUCTION

Pulse-driven ac Josephson voltage standards (ACJVS) have been continuously developed and improved at NIST since 1995 [1-15]. Many improvements have increased performance, including bias techniques [2, 3], error analysis [4-6], junction technology [8], and circuit designs [9, 10]. All of these advancements contributed to increased operating margins and, in particular, output voltages. They also enabled the first 100 mV system with operating range from dc to 100 kHz for rms measurements [11, 12]. More recent improvements have produced a further doubling of the output voltage to 220 mV rms (311 mV peak) [13, 14], which is a 1000-fold increase in output voltage from the original demonstration of 200 µV dc [1]. Other approaches to pulse-driven ac synthesis have been developed by a European Union-funded collaboration [16] and other national measurement institutes [17-19]. The use of a quantum ac voltage source to calibrate thermal transfer standards has been described in [20]. Increasing the rms output voltage to 1 V, as well as increasing the measurement bandwidth to 1 MHz, are challenging goals for future ACJVS systems.

Previous ACJVS research has also focused on reducing potential sources of error [5-7]. For example, by use of an error correction circuit, the ac-ac difference (at 53.4 kHz) was reduced from -176 µV/V to -32 µV/V. A significant improvement in removing low-frequency common-mode error signals was also achieved by using an ac coupling technique [3], which we also used for the measurements in this paper and describe below.

The first 100 mV system was constructed with two Josephson arrays connected in series. We refer to them as "left" and "right" arrays because of their positions on the chip. When measuring these circuits at frequencies above 10 kHz, we found they produced slightly different ac voltages when measured with an ac-dc transfer standard [12]. Kieler, et al. [15] performed extensive measurements of the left and right array ac-dc differences over a frequency range of 2.5 kHz to 100 kHz. They also investigated a number of different wiring configurations, chip designs, and chips from various wafers and fabrication runs. In all cases, the disagreement between the ac-dc differences of the left and right arrays on the same chip was found to increase with increasing frequency. The left-right disagreement at 100 kHz was reduced from the worst case 150 µV/V to only 31 µV/V by changing the chip design, cryoprobe cables, and wiring of the chip.

Two Josephson arrays that are each apparently on operating margins should be well matched. Any disagreement between these arrays is clearly undesirable and suggests the existence of systematic error signals (SES). In this paper, we describe the sources of the systematic errors that produced the left-right array disagreement. Most importantly, we explain how to measure and reduce these error signals below 5 µV/V at 100 kHz.

2. ACJVS BIAS AND CIRCUIT SCHEMATIC

In order to achieve the largest output voltage, two identical Josephson arrays (left and right) were separately biased and their synthesized voltages were added in series so that each array produced half the maximum voltage. Fig. 1 shows the optimum ACJVS wiring configuration, where the arrays are series connected (shorted together) in the room-temperature 'top' of the cryoprobe. This wiring configuration was previously determined to produce the largest operating margins for 220 mV rms circuits [13, 15]. We use the notation: V = voltage, I = current, R = right array, L = left array, LR = both arrays in series, *hi* = high, *lo* = low/ground. Biases and wiring are shown for the right (R) Josephson voltage array (JVA). Those of the left (L) array are similar except for the inverted polarity of both the current compensation (I_L^{comp}) and the output voltage (V_L), the latter due to the inverted Digital Code Generator data. Despite of the left array inverted output voltage polarity, V_L (hi) is close to DCB_{10} (as it is in the right array case). Fig. 1(a) shows the relevant ACJVS bias components, wiring details, and input and output signals. Fig. 1 (b) shows the JVA on-chip circuit schematic, including the low-pass filter (LPF) and some of the inductances present in the circuit. Fig. 1 (c) shows how the two arrays are series connected through the "short-top" wiring configuration (V_R(hi) connected with V_L(hi)) in the top of the cryoprobe.

In order for each array to accurately generate the desired voltage waveform, we need to bias them with two high-frequency (HF) signals and one audio-frequency signal. The HF signals include a continuous wave 15 GHz microwave signal and a broadband two-level digital signal that is produced by a digital code generator (DCG) clocked at 10 Gbps. After these two signals were combined with a microwave coupler, such that it produces a bipolar output waveform, [2] the resulting signal was used to bias the Josephson array. Unfortunately, the broadband digital signal produces a low-frequency common-mode voltage on the microwave-transmission-line termination resistor (R_T). The ac coupling technique mentioned above was devised to remove this common-mode signal so that multiple arrays (two arrays in this paper) can be series connected to increase the output voltage [3]. The output voltage is proportional to the number of junctions; each array has N = 2560 junctions for the 110 mV rms circuits used in the 100 mV rms system. The 220 mV rms circuits have double that number at 5120 junctions per array.

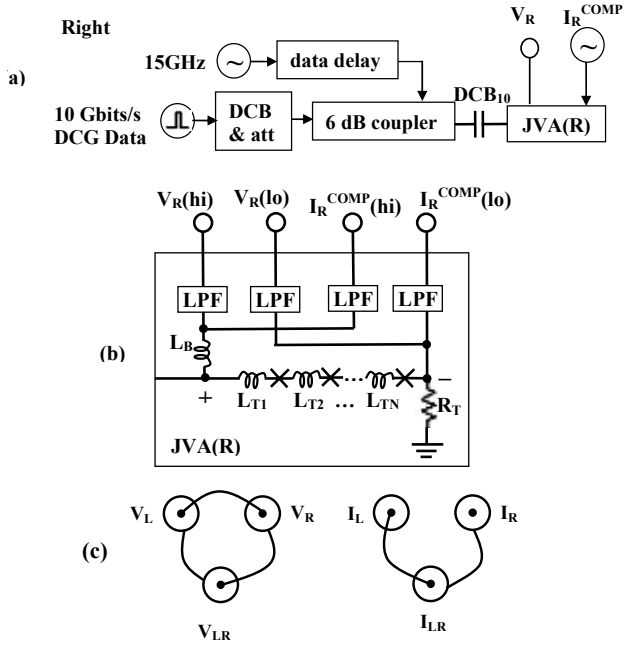

Fig. 1. (a) Biases for the right array JVA(R). (b) On-chip schematic showing relevant circuit parameters for JVA(R). (c) "Short-top" wiring configuration of the ACJVS where BNC centers represent "hi" signal (only three junctions are shown as an example).

DC blocks inside the cryoprobe (DCB_{10} in Fig. 1) have a pass band of 10 MHz to 18 GHz and were used to ac couple the HF signals to the array. These and additional dc blocks attenuate the audio-frequency signals with the expectation that they effectively remove all of the low-frequency common-mode voltage on R_T. However, because the low-frequency part of the digital signal is needed to properly bias the arrays, we separately reapply the low-frequency signals to each array as a current "compensation" I^{comp} through the $I^{comp}{}_R$ and $I^{comp}{}_L$ connections [3]. Because these currents do not flow through R_T, they do not produce a common-mode signal. The compensation signals are generated by arbitrary waveform generators (AWGs) and floating, battery-powered differential amplifiers. All bias sources are phase-locked to a common 10 MHz reference. The AWGs are synchronized to the DCG waveform by use of a pattern trigger.

Additional dc blocks and a 3 dB attenuator ("DCB & att" block) further attenuate the audio frequency signals from the DCG. These are inner-only blocks that have a pass band of 250 MHz to 18 GHz. The attenuators reduce the DCG signal applied to the array as well as damp reflections.

3. MEASUREMENT AND COMPENSATION OF SYSTEMATIC ERROR SIGNALS

We experimentally determined that the dominant systematic-error signals (SES) occur at the frequency of the synthesized waveform. It will be shown that the largest SES, V_{DCG}, is produced by audio-frequency feed through from the DCG caused by inadequate attenuation from the existing dc block configuration. The second most important SES, V_{AWG}, is due to current compensation signals. Both of these current signals drive various inductances whose voltages appear in the voltage measurement path. Each of the signals for the two different arrays, V_{AWG} and V_{DCG}, has different phase angles, φ_1 and φ_2 respectively, relative to the Josephson-synthesized waveform, V_{JJ} (Fig. 2). The obvious inductances driven by the various SES are the total array transmission line inductance L_{Ti} summed for each i^{th} junction and the bias lead inductance L_B, which is shared by the output voltage and current leads (at the high side of the transmission line close to DCB_{10} in Fig. 1). The L_{Ti} between each Josephson junction is a fraction of a picohenry, such that the total transmission line inductance NL_{Ti}, is approximately 3.4 nH for the 110 mV circuits, and double that for 220 mV circuits. The high connections to each array are made through a narrow less than 2 μm diameter superconducting wire such that L_B is very small, less than ~20 pH, and the associated

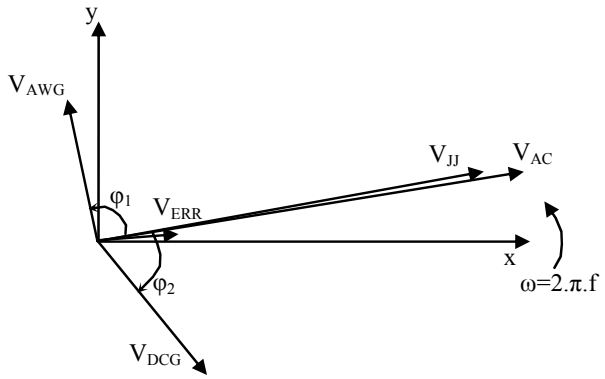

Fig. 2: Vector diagram of the ACJVS voltages. The inferred Josephson signal V_{JJ} and the combined measured output signal V_{AC} are nearly parallel and reduced in scale ~10^5 in order to simplify the figure.

voltage little contributes from either the DCG or AWG biases. However, the DCG SES, in addition to driving the transmission line inductance, may also drive the output voltage and input bias transmission lines through the inductive low-pass filters (LPF). This is done by driving the capacitance that couples the twisted-pair leads of each array (not shown in Fig. 1).

Regardless of exactly where the SES currents are flowing, V_{DCG} and V_{AWG} can be independently measured by reducing their bias amplitudes by 50 % so that the junctions remain in the zero voltage state (not pulsing). In this case, only the inductive or complex impedances are driven and can be measured directly. We measured their magnitudes and phases relative to V_{JJ}. However, since the SES magnitudes are very small compared to the large Josephson voltage, we found that the determination of the phase angles was easier to measure by comparing the SES angles to a lower-amplitude Josephson synthesized-waveform whose amplitude is comparable to the amplitude of ~20 μV rms SES. With this lower voltage amplitude waveform and with the 50 % decreased DCG output amplitude, we can accurately determine the relative phase and amplitude of the DCG error signal.

We measured the magnitude of the SES voltages and combined output voltage V_{AC} with a high-performance precision analog-to-digital converter, a National Instruments PXI-5922 digitizer.[1] We separately measured each signal from each array. The measurements were typically made at the highest frequency (100 kHz) and highest voltage (for each chip) where the SES magnitudes are largest. In order to determine the relative phases of these signals we use as a reference signal the AWG compensation of the opposite array V_{REF}. First, we generate a low-voltage ~20 μV rms ACJVS output signal that has the same phase as the 100 mV rms signal. By design, this signal has exactly the same phase relative to the maximum ACJVS output signal. Next, we adjust V_{REF} to the same amplitude. While measuring both of the signals in series, we adjust the AWG phase (and make minor adjustments to magnitude) to precisely minimize the combined voltage such that V_{REF} is exactly 180° relative to V_{AC}. The resulting AWG phase is used as a reference phase, so that the SES relative phases of the desired maximum output voltage (100 mV rms and 200 mV rms) can be similarly (separately) determined with respect to the measured output voltage.

Fig. 2 shows a vector diagram of the relevant voltages for a single array. The measured voltages are V_{AC}, the effectively measured output voltage; $V_{AWG,}$ the output voltage systematic error signal due to AWG bias of the same array; and, V_{DCG}, the output voltage systematic error due to DCG of the same array. From these measurements, we infer V_{ERR}, which is the sum of V_{AWG} and V_{DCG}. The measured Josephson voltage generated by the array that is inferred from these measurements is $V_{JJ} = V_{AC} - V_{ERR}$.

Since the V_{AWG} is produced by compensation bias applied to primarily inductive components, namely the transmission line inductance (L_{Ti}), it is not surprising that its phase leads that of the output voltage (V_{AC}) by nearly, although not exactly, 90°. On the other hand, the SES signal produced by the DCG bias is attenuated by DC blocks. The specific number and placement of these blocks in the HF transmission line determines the magnitude of the resulting error signal and its phase. This DCG error signal can drive the transmission line inductance and also produce a small common-mode voltage on the termination resistor. The resulting measured DCG SES shows that it typically lags the total ACJVS output voltage. However, as mentioned previously, the magnitude and relative phase will change, depending on the number of blocks that are placed in the transmission line.

Measurements with transfer standards and thermal voltage converters are always rms based. Since V_{JJ} is five orders of magnitude larger than V_{ERR}, the only significant rms contribution of V_{ERR} to the measured voltage V_{AC} is the component that is parallel to V_{JJ}.

There are a number of ways to deal with the SES. We can measure them and account for them in our precision measurements. However, we can also take steps to reduce them by experimental means.

For example, the AWG SES can be reduced by slightly changing the phase angle of the applied current compensation so that it is precisely 90° from V_{JJ} and doesn't contribute to the total rms output voltage. This AWG SES can easily be reduced with only rms measurements by turning on just the AWG signals for a given array (e.g. V_{AWG}(L)) while measuring the total output voltage (e.g. V_{AC}(R)) of the opposite array. We have successfully demonstrated this correction, but have found that the main drawback is that some chips show some reduction in operating margins, from about 2.5 mA peak-to-peak to about 1.3 mA peak-to-peak. Thus, our preferred method is direct measurement and accounting for the rms contribution from V_{AWG}.

Likewise, the DCG SES can be measured and accounted for by using either rms or digitizer measurements. However, once again this signal can be reduced by experimental techniques. A high-pass filter with better stop-band

[1] The commercial instruments are identified in this paper only in order to adequately specify the experimental procedure. Such identification implies neither recommendation or endorsement by the National Institute of Standards and Technology or by Inmetro, nor that the equipment identified is necessarily the best available for the purpose.

attenuation would be preferable to DC blocks for attenuating the audio-frequency signals. Unfortunately, such broadband (10 MHz to 18 GHz) high-pass filters are not easily made with conventional components. Therefore as a practical, although less ideal solution, we added an extra 250 MHz DCB at each DCG output. Additional blocks as well as blocks with higher cut-off frequencies would more effectively attenuate the DCG SES; unfortunately, they can do so at the undesirable expense of reduced operating margins. Thus, there is a compromise between experimental reduction of the SES and maintaining the highest operating margins. When this compromise is met, any remaining SES (especially those for frequencies above 200 kHz) will need to be accounted for mathematically. In our measurements, the addition of one extra 250 MHz DCB at each DCG output doesn't affect the margins. The results of both DCG and SES error reduction techniques are shown below and demonstrate reducing absolute errors from the AWG and DCG signals as well as their associated L-R differences.

4. MEASUREMENTS AND RESULTS

The effectiveness of the techniques for reducing SES described above can be seen in the results of the measurements presented in Table 1. The SES for four different ACJVS circuits (A-D) were measured with the digitizer. They were measured on different days and with different ACJVS circuits. In each case, the bias parameters were adjusted to optimize the operation margins. Once the ACJVS was optimized, each measurement was completed in about 15 minutes. Two chip designs were measured that had different on-chip LPF (18I1 and 18I) and produced 50 mV rms output per array. The 20B designs had twice the number of junctions and each array produced precisely 100 mV rms output. Two different SES reduction techniques were used: (1) *DCB,* where an extra dc block was added to each DCG output to reduce V_{DCG}, and (2) I^{comp}*(angle),* where the AWG current compensation angles were adjusted to reduce V_{AWG} as measured with the transfer standard.

The three first measurements (rows) in Table 1 were made with no SES reduction techniques. Compared to the measurements with SES reduction, they show not only a larger relative SES for each array (left and right) but also a larger relative error difference between the left and right arrays. Even though the magnitudes of V_{AWG} and V_{DCG} are similar, the DCG SES clearly dominates the total combined error as well as the L-R difference because the AWG SES phases are nearly in quadrature to the output signal.

When the additional DCBs are added, the magnitude of V_{DCG} decreases 100-fold and its phase angle shifts 85º. With this reduction technique, the DCG and AWG SES are now of similar magnitude but opposite sign. The margins were not affected by this compensation technique. Note that the L-R difference has decreased only three-fold, even though the absolute DCG error has dropped significantly more. These results emphasize that the L-R difference is an indication of only systematic errors. The above SES measurement techniques are essential for elucidating the absolute errors.

Finally, the last two measurements in Table 1 included both reduction techniques. In this situation, both the absolute errors and the *L-R* difference are the smallest. As could be expected, the I^{comp}*(angle)* technique shifted the

Table 1. Systematic error signal measurements (100 kHz) and inferred Left-Right array differences (rounded values).

Chip	Design	Voltage Per Array, V_{JJ}, (mV)	SES Reduction Technique	Array	V_{AWG}			V_{DCG}			L-R Difference (μV/V)
					Amp (μV)	φ_1 (º)	Error (μV/V)	Amp (μV)	φ_2 (º)	Error (μV/V)	
A 70209n24	18I1	50	———	L	31.3	92.5	-27	31.7	-57.0	345	-62
				R	25.6	90.1	-1	33.0	-54.9	380	
B 70209n33	18I	50	———	L	24.5	92.2	-19	31.0	-56.6	341	-54
				R	26.8	90.5	-5	32.4	-54.0	381	
B 70209n33	18I	50	———	L	23.9	92.1	-18	32.6	-55.5	369	-51
				R	25.5	90.9	-8	34.4	-53.3	411	
C 70129Bn43	20B	100	DCB	L	33.9	94.4	-26	0.5	28.1	5	-18
				R	28.8	91.5	-8	0.5	24.4	4	
A 70209n24	18I1	50	DCB	L	24.3	91.5	-13	0.4	29.7	7	-14
				R	28.9	89.9	1	0.4	30.6	7	
A 70209n24	18I1	50	DCB	L	31.0	91.2	-13	0.3	30.7	5	-12
				R	25.1	90.3	-3	0.4	30.0	7	
B 70209n33	18I	50	DCB	L	27.2	91.9	-18	0.4	32.4	7	-13
				R	26.0	90.5	-5	0.4	31.0	7	
B 70209n33	18I	50	DCB	L	23.8	92.0	-17	0.4	31.0	7	-9
				R	25.5	90.9	-8	0.4	31.5	7	
D 70129Bn34	20B	100	DCB & I^{comp}(angle)	L	27.0	90.4	-2	0.3	-36.4	2	0
				R	28.0	90.5	-2	0.4	31.2	3	
D 70129Bn34	20B	100	DCB & I^{comp}(angle)	L	27.0	89.9	0	0.4	29.0	3	1
				R	28.3	90.1	0	0.4	30.1	3	

relative compensation angles much closer to 90.0^{o} as compared with the previous measurements. The margins were reduced from about 2.5 mA peak-to-peak (typical for 70129Bn34 – 20B design chips) to about 1.3 mA peak-to-peak.

It can be shown that the absolute values of the inferred L-R differences are comparable to those of L-R ac-dc rms differences. We also directly compared the inferred L-R differences to those determined experimentally from ac-dc rms comparisons using the transfer standard. Considering the first measurement in Table 1 (the worse case, chip A without any SES reduction technique), the inferred L-R difference absolute value was 62 μV/V, while the respective measured rms L-R ac-dc difference was 76 μV/V. Similarly, for the last two measurements in Table 1 which used both reduction techniques, the inferred L-R difference absolute values were 0 μV/V and 1 μV/V, while the directly measured L-R rms ac-dc differences were 5 μV/V and 4 μV/V. These results show the consistency of the previous SES measurements as well as the effectiveness of the SES experimental reduction techniques. The ac-dc measurements were performed as described in [15].

5. CONCLUSION

In this paper, we described how to directly measure the intrinsic systematic error signals in the ac Josephson voltage standard. Most importantly, we showed useful techniques for reducing or accounting for these errors. We found that the reduction of these SES using these experimental techniques significantly reduces both the absolute errors as well as the left-right difference errors. For future calibration measurements we plan to reduce the dominant systematic DCG error by using the additional DC blocks. For frequencies up to 100 kHz, we plan to automatically measure and account for the remaining errors. Since we hope to increase the ACJVS bandwidth above 100 kHz in future rms measurements, we expect that measurement and accounting of these errors will be essential.

We believe that the systematic errors described in this paper adequately explain the source of the left-right difference errors that were previously reported. However, further research is required to better understand the remaining frequency-dependent systematic errors in rms measurements that are associated with the output transmission line (and filters) and the input impedance of the transfer standard.

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